Fine Pitch Cu Pillar FC

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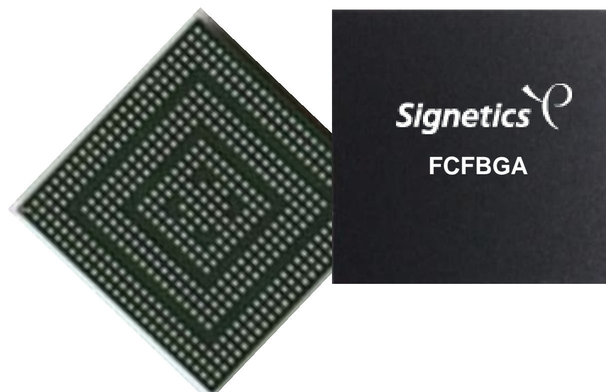

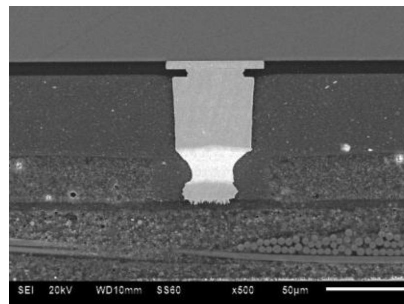

Description

Cu pillar Fc-FBGA Package use Copper(Cu) pillar bump for electrical interconnection. Cu pillar bump is a kind of interconnect between PCB and die. It composes with copper cylinder (Cu post) and mushroom shape solder cap (Solder tip).

Cu pillar bump can not only reduce the die size about 5~10% due to the advantage of fine pitch, but also enhances the thermal and electrical performance , higher reliability, improved electrical than conventional solder material. And it can accomplish to reduce the cost by design factors.

Copper pillar bumps will also help to small fillet requirement for underfill enables more aggressive die-to-package design rule / smaller package footprint.

Package Sizes	6 x 17.1 ~ 14 x 14mm
I/O Counts	34 ~ 409

Features

- Cu pillar with Sn/Ag plated
- 50um to 100um pitch w/ BOF bonding tech.
- Ni-Au, Ni-Pd-Au, SOP (solder on pad), OSP (organic solder preservative), Immersion Tin
- Solder ball : Pb-free solder ball available
- Dispensed underfill (DUF) & Molded underfill (MUF) available
- Supports minimum 0.4mmm ball pitch on bottom pads.
- Packing : JEDEC tray
- Package configuration : JEDEC standards

Applications

- Embedded Processors, Application Processors
- Baseband, ASICs, and Memorys

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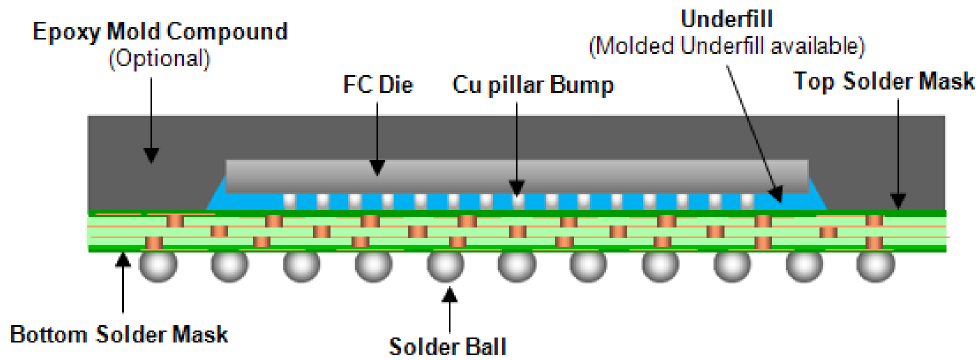
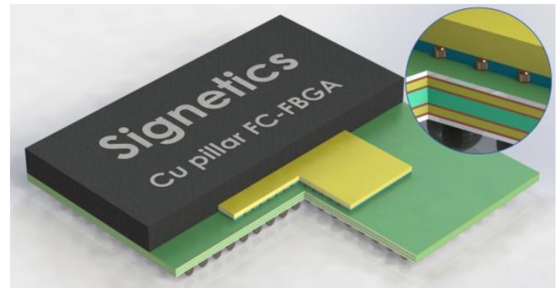


Reliability

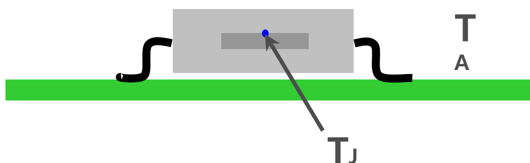
MSL Level	JEDEC Level 3
Temp Cycling	-55°C/125°C, 1000 cycles
Unbiased HAST	130°C/85% RH, 2 atm, 96hrs
High Temp Storage	150°C, 1000hrs



Thermal Data

BODY SIZE	Ball Count	Theta JA (°c/w)
FCFBGA 14X14 Cu pillar	409	21.81

- JEDEC STD 2S2P PCB, Still air

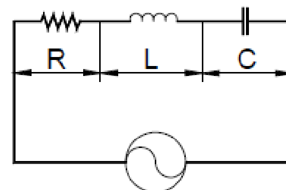


Electrical Data

- 13X13mm Body, 144B
- Simulation Frequency : 2.4GHz

Resistance (mΩ)	450~3060
Inductance (nH)	0.63~5.4
Capacitance (pF)	0.73~2.76

- Results dependent on body size, die size, and Substrate design etc..



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