

## Description

eMUF & LDP has a exposed die. LDP is short for laser drilled package and it is for bottom package of POP. Compared the heat release rate of normal fc-package with eMUF, eMUF is better performance on condition that add a heat slug or air flow on package.

eMUF & LDP offer chip scale capacity for I/Os around 300 or more. These are also available in both thin core laminate substrate technology as well as build up. eMUF & LDP feature thin and small profile, lightweight packages.

And these packages have advantages of electrical and thermal characteristics than conventional wire bonding method.

## Features

- Eutectic, Pb-free & Cu pillar bumps
- Ni-Au, Ni-Pd-Au, SOP (solder on pad), OSP (organic solder preservative), Immersion Tin
- Overall package height 1.0mm to 0.7mm
- Solder ball : Pb-free solder ball available
- Marking : Laser Marking
- Thermally enhanced version with exposed die by Molded underfill
- Available Laser Drilled process for PoP Bottom package .
- Package thickness of max height 0.7mm to 1.0mm available.
- Supports minimum 0.4mm ball pitch on top and bottom pads.
- Packing : JEDEC tray
- Package configuration : JEDEC standards

## Applications

- Handheld or portable electronic devices
- Mobile Processors for smart phones, Tablets, Network AP, Chipsets for peripheral IC's

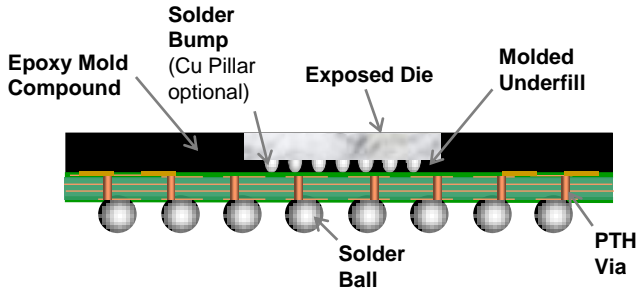
<b>Package Sizes</b>	10 x 10mm – 15 x15mm
<b>I/O Counts</b>	300 – 1296

# fc-FBGA

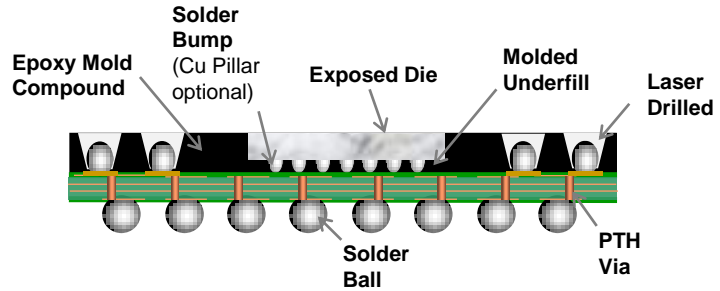
## Exposed MUF / LDP



### eMUF



### LDP



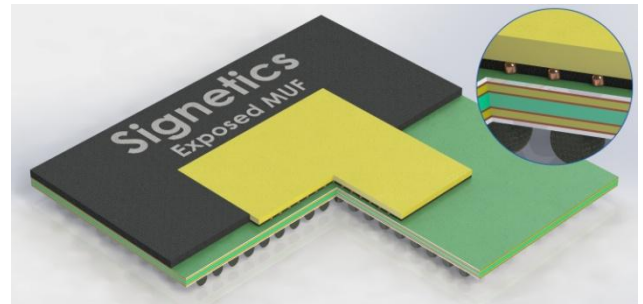
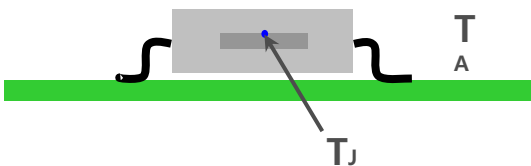
### Reliability

<b>MSL Level</b>	JEDEC Level 3
<b>Temp Cycling</b>	-55°C/125°C, 1000 cycles
<b>Unbiased HAST</b>	130°C/85% RH, 2 atm, 96hrs
<b>High Temp Storage</b>	150°C, 1000hrs

### Thermal Data

BODY SIZE	Ball Count	Theta JA (°C/w)
FCFBGA 10X10 eMUF	100B	27.50

- JEDEC STD 2S2P PCB, Still air

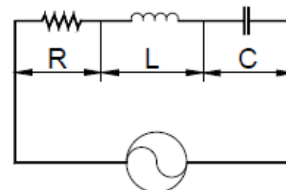


### Electrical Data

- 17X17mm Body, 400B
- Simulation Frequency : 10 GHz

<b>Resistance (mΩ)</b>	1520~4840
<b>Inductance (nH)</b>	3.52~11.85
<b>Capacitance (pF)</b>	0.57~1.38

- Results dependent on body size, die size, and Substrate design etc..



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